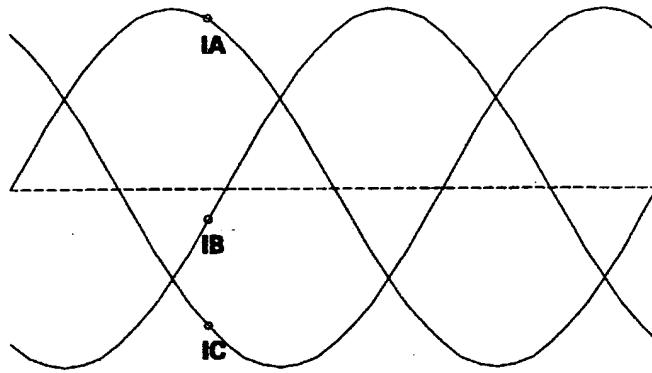


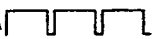
Fig. 1



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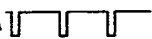
V1A



I1A



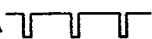
V2A



I2A



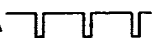
V3A



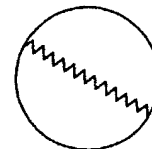
I3A



V4A



I4A



IA DETAIL

V1B



I1B



V2B



I2B



V3B



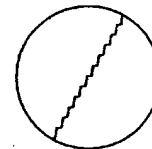
I3B



V4B



I4B



IB DETAIL

V1C



I1C



V2C



I2C



V3C



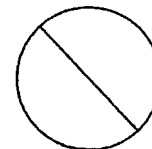
I3C



V4C



I4C



IC DETAIL

Fig. 2



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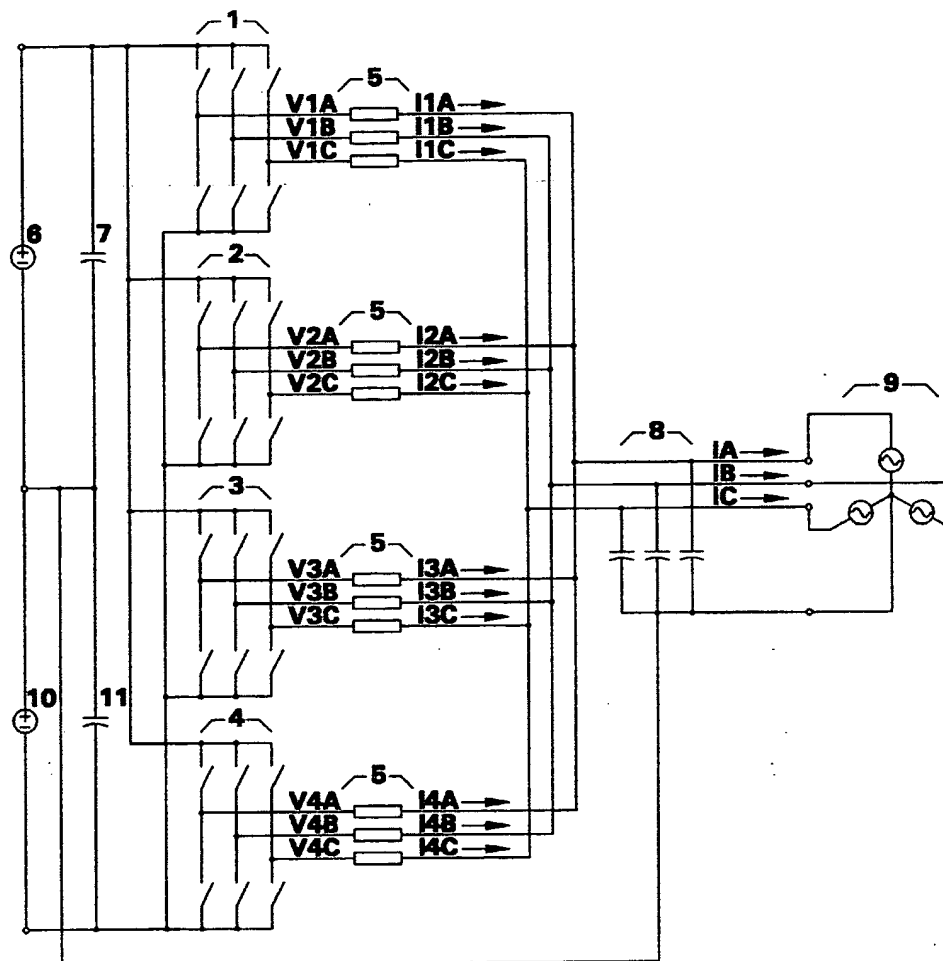


Fig. 3

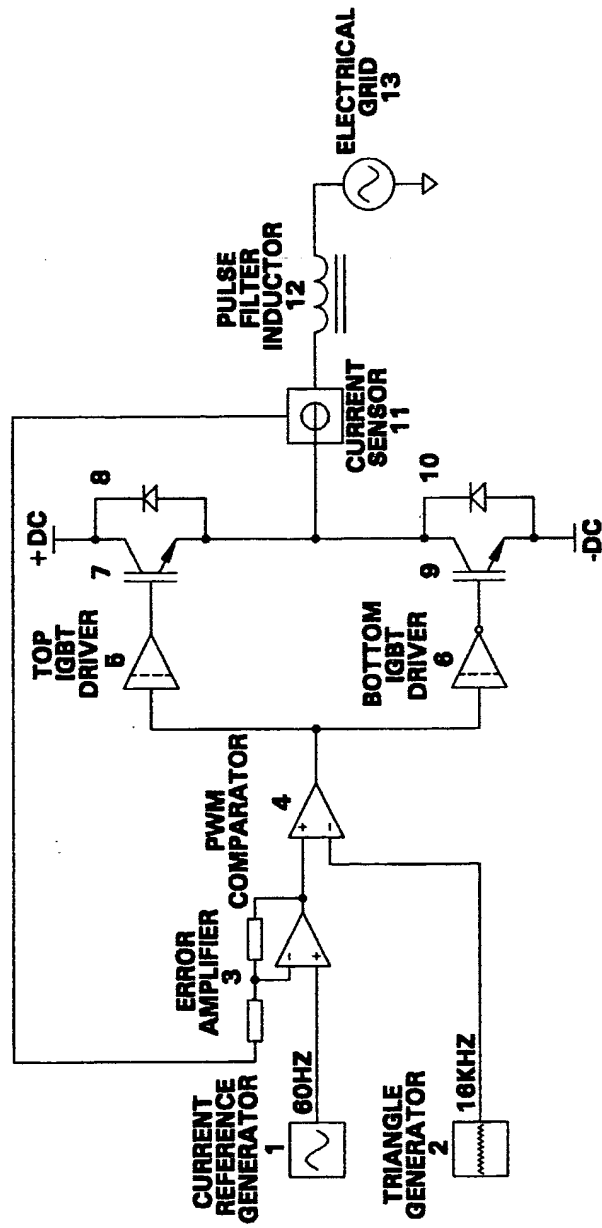


Fig. 4